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D. Remarks

Objections to the Specification

The Specification has been amended to address objections raised in the Office Action, and to address other typographical errors.

Objections to Drawings

With regard to FIGS. 4A and 4B, the figures are believed to be adequately labeled. FIGS. 4A and 4B label item **402** as "NV MEMORY". The specification refers to item **402** as a "first nonvolatile memory". FIGS. 4A and 4B label item **410** as "PROM". The specification refers to this item as a PROM:

> [A] second nonvolatile memory **410** may be a mask programmable ROM...[1]

Therefore, Applicant respectfully requests reconsideration of this ground for objection.

FIG. 4A has been amended to include the reference character **408** referring to the BIST data.

FIGS. 6A to 6C have been amended to include the label NV ELEMENTS pointing to item **606**.

Claim Objections.

Claims 1-9 and 11-16 were objected to for "grammatical informalities". The rejection appears to object to the use of the word "store". Applicant traverses this objection on the grounds that "store" is readily understood. In support of the traversal, Applicant submits a section from The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, as Exhibit A, which provides an entry and definition for "store".

Claim 18 was objected to for grammatical informalities. Applicant respectfully requests clarification of this ground for objection. Claim 18 is believed to meet all statutory requirements for patentability as related to form.

Claim 16 has been amended as suggested by the Examiner.

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[1] See the Specification, Page 11, Lines 18-19.

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Claim 15 has been amended to include the term "store".

Claim 20 was objected to for grammatical informalities. Applicant respectfully requests clarification of this ground for objection. Claim 20 is believed to meet all statutory requirements for patentability as related to form.

Claim Rejections.

Applicant thanks the Examiner for the clear statement for the grounds of rejection.

The rejections of claims 1-10 will first be addressed.

Rejection of Claims 1 and 2 Under 35 U.S.C. §103(a), based on U.S. Patent No. 5,991,907 (*Stroud et al.*) in view of U.S. Patent No. 5,889,701 (*Kang et al.*), further in view of U.S. Patent No. 5,946,267 (*Pathak et al.*).

The invention of amended claim 1 is directed to a programmable logic device (PLD) assembly that can include a programmable logic circuit that provides functions according to configuration data, including a self-test function. Also included is at least one nonvolatile store of the PLD assembly coupled to the programmable logic circuit that provides self-test configuration data for the programmable logic circuit and can subsequently store user configuration data.

As is well known, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.

As noted above, Applicant's claim 1 invention includes at least one nonvolatile store that provides self-test configuration data and can store user configuration data. As originally claimed, and as emphasized by Applicant's amendment, the at least one non-volatile store is part of the same PLD assembly as the programmable logic circuit. The cited combination of references is not believed to not show or suggest such a claim limitation.

The rejection admits that while *Stroud et al.* shows a test controller that retrieves built-in self-test (BIST) configuration data, the reference is silent as to a store being non-volatile[2]. However, Applicant adds that *Stroud et al.* also fails to show any sort of store that is part of a

[2] See the Office Action, dated 4/24/03, Page 4, Lines 7-8.

PLD assembly, as claimed. Further, the teachings of *Stroud et al.* teach away from such a claim limitation.

In *Stroud et al.* BIST configuration data is retrieved from a test controller. The reference describes a test controller as automatic test equipment (ATE), a central processing unit (CPU), or a maintenance processor.[3] Thus, *Stroud et al.* teaches the retrieval of BIST configuration data from an independent piece of equipment separate from the FPGA under test. Consequently, the reference not only does not show Applicant's claim limitation, but teaches away from moving BIST configuration data onto the same assembly as a programmable logic circuit, as set forth in claim 1.

Modifying *Stroud et al.* in view of *Kang et al.* does not arrive at Applicant's claim limitations, either. The rejection proposes modifying the FPGA under test in *Stroud et al.*, with an in-system programmable FPGA as set forth in *Kang et al.*[4] This modification appears to add no additional teachings over *Stroud et al.* *Stroud et al.* teaches the testing and programming of an FPGA already installed in a system that can be programmed "in system"[5]. Still further, *Kang et al.*, teaches away from Applicant's claim limitations, as self-test data, like *Stroud et al.*, is provided by automatic test equipment:

> A standard mainframe tester, an Automated Test Equipment (ATE), is programmed to follow the method of the present invention.[6]

Thus, both *Stroud et al.* and *Kang et al.* teach away from Applicant's claim limitations of "at least one store of a PLD assembly that provides self-test configuration data", by having all test data retrieved on separated ATE.

Modifying *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.* still fails to show Applicant's claim 1 limitations. *Pathak et al.* discloses a configuration memory that can initialize a programmable logic device. However, *Pathak et al.* provides no mention of (1) such a configuration memory being part of an assembly that includes a programmable logic circuit or

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[3] See *Stroud et al.*, Col. 4, Lines
[4] See the Office Action, dated 4/24/03, Page 4, "Combination A".
[5] See *Stroud et al.*, Col. 7, Lines 46-52.
[6] *Kang et al.*, Col. 2, Lines 22-23.

(2) such a memory storing self-test data for the programmable logic circuit. Accordingly, the reference cannot be suggestive of Applicant's claim 1 limitations.

Thus, the cited combination of references does not show or suggest Applicant's claim 1 limitations.

For all of these reasons, a prima facie case of obviousness is not believed to have been established for this case, and this ground for rejection is traversed.

Rejection of Claim 3 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of U.S. Patent No. 6,044,025 (*Lawman*).

To the extent that this ground of rejection relies on the combination of *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, the comments set forth above for claims 1 and 2 are incorporated by reference herein. Namely, that the combination does not present a prima facie case of obviousness for the base claim limitations.

It is additionally noted that *Lawman*, like *Stroud et al.* and *Pathak et al.*, emphasizes testing via configuration data stored in a tester[7] – once again teaching away from Applicant's claim 1 limitations.

Rejection of Claim 4 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of U.S. Patent No. 6,046,957 (*Shyu*).

Claim 4, which depends from claim 1, recites that at least one nonvolatile store includes a first nonvolatile store formed with the programmable logic circuit on a single integrated circuit die.

To the extent that this ground of rejection relies on the combination of *Stroud et al./Kang et al./Pathak et al.*, the comments set forth above for claims 1 and 2 are incorporated by reference herein. Namely, that the combination does not present a prima facie case of obviousness for the base claim limitations.

In addition, the references do not provide the suggestion/motivation to modify *Stroud et al./Kang et al./Pathak et al.* in view of *Shyu*, as proposed. As indicated above, the reference only teaches self-test configuration data being included on a tester, or the like. The incorporation of

[7] See *Lawman*, Col. 1, Lines 55-57

tester functions into a system-on-a-chip (SOC) is beyond the suggested teachings of *Shyu*. In describing SOC trends, *Shyu* states the following:

> With the growing trend toward SOC (system-on-a-chip) technology, it is inevitable to incorporate a variety of circuit building blocks... onto a single integrated circuit chip... [A]n IP (intellectual property) based design approach is performed. The IP-based design approach involves the use of circuit building blocks having specific functions that are well proven for the integration of the system chip.[8]

Applicant asserts that a tester, as taught in *Stroud et al.* and *Kang et al.*, is not a circuit building block – and would not be considered obvious to include in an SOC.

Further, the rejection has not indicated how or if a nonvolatile store and programmable logic circuit are well proven for integration, as required by *Shyu*. Absent such a teaching, there is not motivation modify the references as proposed. It is additionally noted that *Shyu* provides no mention of programmable logic, thus cannot provide the requisite suggestion/motivation for the proposed combination.

For all of these reasons, a prima facie case of obviousness has not been established for claim 4, and this ground for rejection is traversed.

Rejection of Claims 5 and 6 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of U.S. Patent No. 4,771,399 (*Snowden et al.*).

To the extent that this ground of rejection relies on the combination of *Stroud et al./Kang et al./Pathak et al.*, the comments set forth above for claims 1 and 2 are incorporated by reference herein. Namely, that the combination does not present a prima facie case of obviousness for the limitations of base claim 1.

Further, to the extent that this ground of rejection relies on the combination of *Stroud et al./Kang et al./Pathak et al./Shyu*, the comments set forth above for claim 4 are incorporated by reference herein. Namely, that the combination does not present a prima facie case of

[8] *Shyu*, Col. 1, Lines 9-20, emphasis.

obviousness for the limitations of base claim 4.

Rejection of Claims 7 and 8 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of *Cook, Nigel P.*, A First Course in Digital Electronics, Prentice-Hall, 1999 pp. 684-689 (*Cook*).

The rejection of claim 7 will first be addressed.

Claim 7, which depends from claim 4, recites that self-test configuration data on the at least one nonvolatile store is set by a manufacturing process step for a PLD assembly. Thus, the manufacturing step is directed to particular data: self-test configuration data.

The cited combination of references does not show such a limitation. In *Stroud et al.*, BIST configuration data is not set by, or related to, any manufacturing step for a PLD, as such data is maintained on a tester. *Kang et al.* is unrelated to self-test configuration data, and thus cannot be suggestive of Applicant's claim 7 limitation. *Pathak et al.*, *Shyu*, and *Cook* provide no teachings regarding self-testing.

Accordingly, the combination of references cannot arrive at the limitations of claim 7.

Claim 8, which depends from claim 7, recites that at least one nonvolatile store includes a mask programmable read-only-memory (PROM) that stores self-test configuration data and a separate nonvolatile memory that can store user configuration data.

Applicant traverses the rejection of claim 8 based on a number of reasons.

First, the comments above for claim 7 are incorporated by reference herein.

Second, the references do not show or suggest the limitations of claim 8. Applicant's request clarification of how/where the combination of *Stroud et al./Kang et al./Pathak et al./Shyu/Cook* show the limitations of claim 8, as the references all teach single memories for configuration data, and not separate non-volatile memories.

Third, the rationale relied upon in rejecting claim 8 appears to be without basis. The rejection of claim 8 relies on the following reasoning.

> [I]t would have been obvious for a person of ordinary skill in the art to provide a separate non-volatile memory that is programmable after manufacturing for storing user configuration data... The motivation for doing so would be to allow the user to change the user-configuration of the programmable logic device after

> manufacturing, while leaving the self-test configuration data in the MROM since it does not need to be changed after initial design prototyping of the programmable logic device...[9]

Applicant's request clarification of where such a teaching is found in the cited references - as Applicant has reviewed the reference in detail and has found no such teaching. The above rationale appears to be a piecemeal reconstruction of the invention with the benefit of hindsight, and thus is improper.

If it is being argued that the above modification to the references is well known (e.g., established by official notice), Applicant respectfully requests citation of a reference in support of such action.

Rejection of Claims 9 and 10 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of *Snowden*, yet further in view of U.S. Patent No. 5,668,816 (*Douskey et al.*), and yet further in view of U.S. Patent No. 5,032,533 (*Gill et al.*).

Claim 9, which depends from claim 1, recites that at least one nonvolatile store includes at least two sectors and self-test configuration data is stored in a first sector.

To the extent that this ground of rejection relies on the combination of *Stroud et al./Kang et al./Pathak et al.*, the comments set forth above for claims 1 and 2 are incorporated by reference herein. Namely, that the combination does not present a prima facie case of obviousness for the base claim limitations.

The rejection admits that the combination of *Stroud et al./Kang et al./Pathak et al./Shyu/Snowden/Douskey et al.* does not show the limitations of claim 9[10]. To show such limitations, the rejection relies on the following reasoning.

> The motivation for making this modification [modifying *Stroud et al./Kang et al./Pathak et al./Shyu/Snowden/Douskey et al.* in view of *Gill et al.*] would be to simplify re-programming of a logic configuration by placing a single user

[9] See the Office Action, dated 4/24/03, Page 9, Line 22 to Page 10, Line 2.
[10] See the Office Action, dated 4/24/03, Page 12, Lines 5-8.

> configuration in each flash memory block (i.e. sector). Thus, realizing the advantage of allowing one programmable logic configuration to be reprogrammed without affecting the other logic configuration.[11]

Applicant's request clarification of where this teaching can be found in the cited references - as Applicant has reviewed the references in detail and has found no such teaching. If it is being argued the above modification to the references is well known (e.g., established by official notice), Applicant respectfully requests citation of a reference in support of such a claim.

Still further, the above rationale cannot show or suggest why self-test configuration data would be stored in one sector, as self-test data is not mentioned.

This ground for rejection is also traversed on the basis that there is no motivation to combine *Douskey et al.* with the combination *Stroud et al./Kang et al./Pathak et al./Shyu/Snowden*. *Stroud et al.* teaches the drawbacks of including BIST circuits in a device:

> [A]dditional test... circuits increase complexity and space requirements... typically... between 10-30% and significant delay penalties in operating speed...[12]

In contravention to the explicit teachings of *Stroud et al.*, *Douskey et al.* purposely adds BIST circuits to an integrated circuit.[13] Thus, because the teachings of the reference teach against the combination of *Douskey et al.* with *Stroud et al.*, motivation for the proposed combination is lacking and/or any prima facie case of obviousness has been rebutted.

For all of these reasons, this ground for rejection is traversed.

The rejections of claims 11-17 will now be addressed.

Rejection of Claim 11 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of *Snowden et al.*

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[11] See the Office Action, dated 4/24/03, Page 13, Lines 6-11.
[12] *Stroud et al.*, Col. 1, Lines 34-40.
[13] See *Douskey et al.*, FIGURE 1, which shows BIST circuit 104 on the integrated circuit chip 100.

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Claim 11 has been amended to include limitations of claim 16. The invention of amended claim 11 is directed to a method that includes performing a self-test on a programmable logic circuit of one package according to self-test configuration data in a self-test nonvolatile store of the one package. The method also includes storing user configuration data in a user nonvolatile store if the programmable logic circuit passes the self-test.

To address this ground of rejection, Applicant incorporates by reference the same general comments set forth for claims 1 and 2. Namely, just as the combination of *Stroud et al./Kang et al./Pathak et al.* does not show a programmable logic circuit and nonvolatile store of the same PLD assembly, the combination does not show a self-test on a programmable logic circuit according to self-test configuration data in a self-test nonvolatile store, where the programmable logic circuit and self-test nonvolatile store are of the same package.

Accordingly, a prima facie case of obvious has not been established for this claim.

In addition, Applicant's reiterate comments set forth above for claim 9 and 10: *Stroud et al.* teaches the drawbacks of including BIST circuits in a device, which is in opposition to *Douskey et al.*, which purposely adds BIST circuits to an integrated circuit. Thus, motivation for the proposed combination is lacking and/or any prima facie case of obviousness has been rebutted.

For all of these reasons, this ground for rejection is traversed.

Rejection of Claims 12-15 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of *Snowden*, still further in view of *Douskey et al.*

To the extent that this ground of rejection relies on the combination of *Stroud et al./Kang et al./Shyu/Snowden*, the comments set forth above for claim 11 are incorporated by reference herein. Namely, that the combination of references do not show all limitations of base claim 11.

In addition, with respect to claim 14, this claim recites storing user configuration data in locations that are different than those that store self-test configuration data. To address this rejection, Applicant incorporates the same general comments set forth above for claims 9 and 10. Namely, that rationale relied upon does not appear to be derived from the references.

With respect to claim 15, this claim recites forming a self-test nonvolatile store on the same die as the programmable logic circuit. To address this ground of rejection Applicant

incorporates by reference herein the same general comments set forth above for claim 4. Namely, that the reference do not show or suggest the limitations of claim 15.

Rejection of Claims 16 and 17 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of *Snowden*, still further in view of *Douskey et al.*, in view of U.S. Patent No. 5,909,587 (*Tran*).

To the extent that this ground of rejection relies on the combination of *Stroud et al./Kang et al./Shyu/Snowden*, the comments set forth above for claim 11 are incorporated by reference herein. Namely, that the combination of references do not show all limitations of base claim 11.

In addition, this ground of rejection is traversed on a number of additional reason.

There is no motivation to add *Tran* to the above combination as the reference teaches away from the express teachings of *Shyu*. The teachings of *Shyu* are directed to combining well proven circuit blocks for integration into a single system chip (SOC). *Tran*, in express contravention to the teachings of *Shyu*, is directed to separating functions into different chips.

Thus, because the *Tran* teaches away from the proposed modification, the requisite suggestion/motivation for a prima facie case of obvious has not been established, or any prima facie case of obviousness has been rebutted.

Rejection of Claims 18 and 19 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of *Snowden*, still further in view of *Douskey et al.*

Claim 18 has been amended to include the limitations of claim 1. Amended claim 18 is directed to a programmable logic assembly self-test method that includes the steps of: storing self-test information in a first nonvolatile store of the assembly that places a programmable logic circuit of the assembly into a self-test configuration; executing a self-test on the programmable logic circuit; and providing user configuration information that places the programmable logic circuit in a user configuration.

To address this ground for rejection the same general comments set forth above for claims 1 and 2 are incorporated by reference herein. Namely, that the cited references are directed to arrangements in which self-test is resident on a tester, not a nonvolatile store of an assembly.

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Rejection of Claim 20 Under 35 U.S.C. §103(a), based on *Stroud et al.* in view of *Kang et al.*, further in view of *Pathak et al.*, and even further in view of *Shyu*, yet further in view of *Snowden*, still further in view of *Douskey et al.*, yet further in view of U.S. Patent No. 5,759,877 (*Crafts et al.*)

Claim 20, which depends from claim 18, includes user configuration data being stored in a second nonvolatile store that is different than the first nonvolatile store. The rejection of this claim relies on the following reasoning.

> The motivation for doing so [modifying *Stroud et al./Kang et al./Pathak et al./Shyu/Snowden/Douskey et al.* in view of *Crafts et al.*] would be to prevent the self-test data from being overwritten unintentionally by the user when user configuration data is programmed.[14]

Applicant's request clarification of where this teaching can be found in the cited references - as Applicant has reviewed the reference in detail and has found no such teaching. If it is being argued the above modification to the references is well known (e.g., established by official notice), Applicant respectfully requests citation of a reference in support.

Thus, because the rejection appears to rely on a teaching not set forth in cited reference, a prima facie case of obviousness has not been established for this claim, and this ground for rejection is traversed.

[14] See the Office Action, dated 4/24/03, Page 18, Lines 1-2.

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Claims 1-2, 7-8, 11, 14-16 and 18 have been amended. The present claims 1-20 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

7/22/03

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EXHIBIT A

Excerpts from

The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition

For Serial No.: 09/602,938
Applicant(s): MOORE, Michael

IEEE 100
The Authoritative Dictionary of IEEE Standards Terms

Seventh Edition

IEEE
Publish d by
Standards Information Network
IEEE Press

stop list.
g or wading pool A pool with
ft and a maximum wall height
at it may be readily disassembled
to its original integrity.
(NESC)
ectronic computation) The
(electronic computation)
n can be stored, sometimes called
tronic computation) In a comput
ly for storing information
a memory or store (British)
f storing information may be el
gnetic, acoustic, optical,
echanical, etc., in nature. 2.
ata can be entered, in which it
t can be retrieved at a later
(MIL/C)
rement) In a computer, one
ore data. (C)
ition of data in a storage dev
data into a storage device. (C)
edium in which data can be
(C)
access.
(1) (computers) The assign
instructions to specified
(C)
element of computer resource
ning storage areas to specific
ocedures, such as transfer of
storage, to support the assig
uffer; contiguous allocation;
elay; memory compaction;
(C)
'orage tubes) An assembly
that contains the target toget
trol of the storage process;
nal,' and other members used
storage tube. (BD)
ttery comprised of one
d-acid, nickel-cadmium, or
il types. (NESS)
'see: data breakpoint.
low leakage capacitor on
(C)
The amount of data that can
Notes: 1. The units of capac
etc. For example, capacity
mal digits," "16 384 words
ers each." 2. When comparing
ing different character sets
nvenient to express the capac
the number obtained by
of the number of usable
torage can exist. 3. The
mputer usually refers only to
(C)
maximum number of items
ge device; usually measured
(C)
ata that can be contained
binary characters, bytes,
(C)
'ata that can be contained
(BD)
ic energy) (secondary cell
d for the generation of
being discharged, may be
ion by an electric current
the flow of current when

One or more storage elements considered as a unit.
smallest subdivision of storage into which a unit of
be placed, retained, and with which the unit can be
Synonym: data cell. *See also:* binary cell; magnetic
(C) 610.10-1994
elementary unit of storage (e.g., a binary cell or a
cell). (ED/C) 1005-1998, [85], [20]
channel A channel that can be used to access a storage
(C) 610.10-1994w
device (1) A device in which data can be stored and
which it can be copied at a later time. The means of
data may be chemical, electrical, mechanical, etc. *See*
storage. (C) 162-1963w
device into which data can be placed, in which they can
ained, and from which they can be retrieved. *See also:*
(C) 610.10-1994w
display *See:* storage tube display device.
efficiency The degree to which a system or component
its designated functions with minimum consump-
available storage. *See also:* execution efficiency.
(C) 610.12-1990
element (1) (storage tubes) An area of a storage sur-
that retains information distinguishable from that of ad-
areas. *Note:* The storage element may be a portion of
inuous storage surface or a discrete area such as a di-
island. *See also:* storage tube.
(ED) 158-1962w, 161-1971w
basic unit of a storage device, such as a sector, or a
(C) 610.10-1994w
element equilibrium voltage (storage tubes) A lim-
oltage toward which a storage element charges under
dition of primary electron bombardment and secondary
on. At equilibrium voltage the escape ratio is unity.
Cathode equilibrium voltage, second-crossover equilib-
voltage, and gradient-established equilibrium voltage
ical examples. *See also:* charge-storage tube.
(ED) 158-1962w
element equilibrium voltage, cathode (storage tubes)
orage element equilibrium voltage near cathode voltage
below first-crossover voltage. *See also:* charge-storage
(ED) 158-1962w
element equilibrium voltage, collector *See:* charge-
tube.
element equilibrium voltage, gradient established
ge tubes) The storage-element equilibrium voltage, be-
first- and second-crossover voltages, at which the ca-
ratio is unity. *See also:* charge-storage tube.
(ED) 158-1962w
element equilibrium voltage, second-crossover (stor-
tubes) The storage-element equilibrium voltage at the
d-crossover voltage. *See also:* charge-storage tube.
(ED) 158-1962w
error An error in which the data retrieved from storage
ifferent from that which was originally stored in that lo-
See also: soft error; hard error; transient error.
(C) 610.10-1994w
id (microprocessor operating systems parameter
An identifier for a block of data. The identifier is not
ended to be valid outside the allocating process and
not be passed between processes.
(C/MM) 855-1985s
integrator In an analog computer, a device used to store
tage in the hold condition for future use. *See also:* elec-
analog computer. (C) 610.10-1994w, 165-1977w
life (accelerometer) (gyros) (inertial sensors) The
perating time interval under specified conditions, after
ch a device will still exhibit a specified operating life and
rmance. *See also:* operating life.
(AES/GYAC) 528-1994
light A light found on a storage device indicating that
rity check error has occurred on a character as it was read
(C) 610.10-1994w

storage light-amplifier *See:* image-storage panel.

storage location (1) An area in a storage device that can be explicitly and uniquely specified by means of an address. (C) 610.5-1990w

(2) A location in a storage device that is uniquely specified by means of an address. (C) 610.10-1994w

storage medium Any device or recording medium into which data can be stored and held until some later time, and from which the entire original data can be obtained. (IA) [61]

storage protection (computers) An arrangement for preventing access to storage for either reading or writing, or both. (C) [20]

storage rate The frequency with which sampled signals are recorded in crashworthy nonvolatile memory. The event recorder may store any signal less often than it samples. (VT) 1482.1-1999

storage, reservoir *See:* reservoir storage.

storage schema In a CODASYL database, statements expressed in data storage definition language that describe storage areas, stored records, and any associated indices and access paths supporting the records and sets defined by a given schema. *See also:* CODASYL database. (C) 610.5-1990w

storage stack *See:* stack.

storage station (power operations) A hydroelectric generating station associated with a water storage reservoir. (PE/PSE) 858-1987s, 346-1973w

storage structure (A) The manner in which data structures are represented in storage. (B) The configuration of a database resident on computer storage devices after mapping the data elements of the logical structure of the database onto their respective physical counterparts. *Note:* The relationships and associations that provide the physical means for accessing the information stored in the database are preserved. (C) 610.5-1990

storage surface (storage tubes) The surface upon which information is stored. *See also:* storage tube. (ED) 158-1962w

storage temperature (1) **(power supply)** The range of environmental temperatures in which a power supply can be safely stored (for example, −40°C to +85°C). (AES/IA) [41], [12]

(2) **(light-emitting diodes)** The temperature at which the device, without any power applied, is stored. (ED) [127]

storage temperature range The range of temperatures over which the Hall generators may be stored without any voltage applied, or without exceeding a specified change in performance. (MAG) 296-1969w

storage time *See:* decay time; maximum retention time.

storage tube An electron tube into which information can be introduced and read at a later time. *Note:* The output may be an electric signal and/or a visible image corresponding to the stored information. (ED) 161-1971w, 158-1962w

storage tube display device A type of cathode ray tube display device that retains a display image on its surface in the form of a pattern of electric charges. *Synonyms:* storage display; display storage tube; direct-view storage tube. *Contrast:* refresh display device. (C) 610.10-1994w

storage unit The length of an addressable element of storage in the machine, measured in bits. (Every storage element has the same size.). *Note:* The storage unit is very likely to be one byte, but this is not a requirement. For example, it might be 32 or 64 bits. (C) 1003.5-1999

store (A) A device into which data can be placed, in which they can be retained, and from which they can be retrieved. *Note:* This term is the equivalent of the term storage in British (U.K.) usage. (B) To place data into a device as in definition (A). (C) To retain data in a device as in definition (A). (C) 162-1963, 610.10-1994

(2) (A) To place or retain data in a storage device. (B) (software) (data management) To copy computer instructions or data from a register to internal storage or from internal storage to external storage. *Contrast:* retrieve; load. *See also:* move; fetch. (C) 610.12-1990, 610.5-1990